REMARKS

This is a full and timely response to the Final Office Action (Paper No. 4) mailed by the U.S. Patent and Trademark Office on March 4, 2003.

Applicant thanks the Examiner for acknowledging acceptance of the drawing corrections and corresponding substitute drawings submitted December 30, 2002.

Upon entry of the attached amendments, claims 1, 4-6, and 11 have been amended. Claims 1, 4-6, and 11 are hereby amended to more particularly point out and distinctly claim the subject matter that Applicant regards as the invention. The subject matter recited in the amended claims was submitted in the preamble of corresponding claims as originally submitted. Consequently, Applicant submits no new matter is added.

Each rejection presented in the Final Office Action is discussed in the remarks that follow.

Reconsideration of the pending claims is respectfully requested, in view of the preceding amendments and the following remarks.

I. Response to 35 U.S.C. §102 Rejections – Claims 1-3

A. Statement of the Rejection

Claims 1-3 presently stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Roussel et al. (U.S. Patent Number 6,230,257 "the '257 patent.")

B. The '257 Patent

The '257 patent is directed to a method and apparatus for staggering execution of an instruction. According to one embodiment of the invention, a single macro instruction is received wherein the single macro instruction specifies at least two logical registers and wherein the two logical registers respectively store a first and second packed data operands having corresponding data elements. An operation specified by the single macro instruction is then performed independently on a first and second plurality of the corresponding data elements from said first and second packed data operands at different times using the same circuit to independently generate a first and second plurality of resulting data elements. The first and second plurality of resulting data elements are stored in a single logical register as a third packed data operand. (U.S. Patent 6,230,257 column 2, lines 26-40).

C. Discussion of the Rejection

Applicant respectfully traverses the rejection of claims 1-3 under 35 U.S.C. §102(e) for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claims. It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of *each element* of the claim under consideration." *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983) (*emphasis added*). Therefore, every claimed feature and each of its limitations must be represented in the applied reference (the '257 patent) to constitute a proper rejection under 35 U.S.C. §102(e).

For convenience of analysis, independent claim 1, as amended, is repeated below in its entirety.

> 1. An apparatus, comprising:
> ***a single multiply accumulate (MAC) unit configured to generate a data result responsive to a single-instruction multiple-data (SIMD) instruction, the data result having a first half and a second half***;
> ***a register communicatively coupled to the single MAC unit, the register configured to store the first half of the data result***; and
> ***a miscellaneous-logic unit configured to initiate the release of the first half of the data result from the register to synchronize the first half of the data result with the second half of the data result.***

(Applicant's amended independent claim 1 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized elements of pending claim 1 as shown above. Consequently, claim 1 is allowable.

In this regard, the Office alleges, "Roussel et al. have taught an apparatus for performing single instruction multiple data instructions using a single multiply accumulate (MAC) unit . . .said MAC unit generates a first half of a data result and a second half of a data result (Figure 3, column 3, lines 21-43, the first half, or low order, of the data result is (x1+y1)(x0+y0), the second half, or higher order, of a data result is (x3+y3)(x2+y2), which are both generated from a MAC unit); . . ." Applicant respectfully disagrees that the '257 patent teaches using a single MAC unit to perform a

SIMD operation. The Office Action's interpretation of what is allegedly disclosed in the '257 patent is in direct contradiction with the following statement from the '257 patent.

> Thus, according to an embodiment of the present invention, ***execution units*** *are provided that contain only half the hardware* ***(e.g. two single precision ADD execution units and two single precision MUL execution units)***, instead of the execution units required to process the full width of the operands in parallel as found in a current processor.

(U.S. Patent 6,230,257, column 4, lines 59-64, *emphasis added.*)

The system apparently disclosed in the '257 patent describes two single-precision ADD-execution units and two single-precision MUL-execution units. Two single-precision ADD-execution units and two single-precision MUL-execution units *are not* a single MAC unit as the Office Action rejection suggests.

The Office Action, in addressing Applicant's response submitted December 30, 2002, offers that column 3, lines 39-41 indicates that other execution units such as FMAC units may be used. Based on this statement alone, the Office Action alleges that the '257 patent teaches Applicant's apparatus. Applicant respectfully disagrees. The standard for anticipation, as recited above, requires that each element and all its limitations be disclosed in a single prior-art reference. The '257 patent fails to describe a single MAC unit configured in combination with the other recited elements as claimed. Consequently, for at least this reason, the '257 patent fails to disclose, teach, or suggest Applicant's claimed invention.

Furthermore, Figures 4A and 5 of the '257 patent illustrate the use of delay elements (M1, M2, and M3 in Figure 4A and M 190, M 200, and M 400 in Figure 5) apparently for delaying the transmission of a portion of a data word to an execution unit. Clearly, the apparatus apparently disclosed in the '257 patent is different from Applicant's claimed invention in this regard. The apparatus of the '257 patent uses passive delay elements arranged to intercept data as it is clocked to the plurality of execution units. In contrast, Applicant's claimed invention recites "***a register communicatively coupled to the MAC unit, the register configured to store the first half of the data result; . . . ; and a miscellaneous-logic unit configured to initiate the release of the first half of the data result from the register.***" Passive delay units

arranged to intercept data bytes on their way to an execution unit *do not* teach a register coupled to a MAC unit configured to store a data result.

The Office Action, in addressing Applicant's response submitted December 30, 2002, offers that the delay elements of the '257 patent store a value that is read later. Applicant respectfully disagrees. The circuits apparently disclosed in FIGs. 4A and 5 of the '257 patent show delay elements coupled to execution units via multiplexers. The passive delay elements and bypass control logic apparently disclosed in the '257 patent forward data in accordance with a clock signal and a destination control input. The circuits shown in FIGs. 4A and 5 simply forward and route data values. Once the data processing operation is initiated, data is forwarded to the ADD and MUL execution units as directed by the clock signal. Thus, the circuit elements apparently disclosed in FIGs. 4A and 5 cannot store a data result that is later controllably released in response to a miscellaneous logic unit.

In contrast, Applicant's independent claim 1 includes "***a register communicatively coupled to the MAC unit, the register configured to store the first half of the data result; . . ; and a miscellaneous-logic unit configured to initiate the release of the first half of the data result from the register to synchronize the first half of the data result with the second half of the data result.***" A register consists of a group of flip-flops and logic gates that effect their transition. The flip-flops hold binary information while the logic gates control when and how the binary information is transferred into the register. After data is stored in the register, the data can be "read" and/or applied multiple times to circuit elements coupled to the output of each respective flip-flop. The standard for anticipation, as recited above, requires that each element and all its limitations be disclosed in a single prior-art reference. The '257 patent fails to describe a single MAC unit configured in combination with the other recited elements as claimed. Consequently, for at least this reason, the '257 patent fails to disclose, teach, or suggest each element of the Applicant's claimed invention.

Accordingly, for at least these reasons, Applicant respectfully submits that Applicant's claim 1 and each dependent claim that depends therefrom are allowable over the '257 patent. Applicant therefore requests that the rejection of claims 1-3 be withdrawn.

VII. Response to 35 U.S.C. §103 Rejections – Claims 4-15

A. Statement of the Rejection

Claims 4-15 presently stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Roussel et al. (U.S. Patent No. 6,230,257) "the '257 patent") in view of Phillips et al. (U.S. Patent No. 6,038,652, "the '652 patent.") Concerning claim 4 the Office Action rejection acknowledges that the '257 patent is silent regarding a miscellaneous logic unit generating an exception result when the miscellaneous logic unit determines that the first half of the data result is in error. To remedy this admitted failure of the '257 patent to disclose, teach, or suggest each element of the claimed invention, the Office Action alleges the '652 patent teaches that overflow or other exceptions may occur during multiply and accumulate functions and that it is necessary to report the exception so that appropriate action may be taken. The rejection then concludes it would have been obvious to one skilled in the art at the time of the invention to modify the system of the '257 patent to generate and report an exception.

B. The '652 Patent

The '652 patent is directed to a method and apparatus for reporting exceptions in a single instruction multiple data (SIMD) processor in computing an arithmetic function for a plurality of argument data. The SIMD processor is configured for processing *N* elements simultaneously. A sequence of instructions is re-arranged to allocate the plurality of argument data in the *N* elements. The *N* elements are processed simultaneously. The exceptions for *N* elements are detected simultaneously. The detected exceptions are then combined to generate a global exception. (U.S. Patent 6,038,652, Abstract.)

C. Discussion of the Rejection

1. Claims 4 and 5

Applicant respectfully traverses the rejection of claims 4 and 5 under 35 U.S.C. §103(a) for at least the reason that even the proposed combination of references fails to disclose, teach, or suggest each element in the claims.

As pointed out above, the '257 patent fails to teach element of Applicant's independent claim 1. Thus, modifying the apparatus of the '257 patent to add exception

handling as the Office Action suggests fails to remedy the failure of the '257 patent to disclose, teach, or suggest Applicant's claimed apparatus. Because independent claim 1 is allowable, dependent claims 4 and 5 are also allowable. *See In re Fine*, 837, F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Accordingly, Applicant respectfully requests that the rejection of claims 4 and 5 be withdrawn.

2. Claims 6-10

Applicant respectfully traverses the rejection of claims 6-10 under 35 U.S.C. §103(a) for at least the reason that even the proposed combination of references fails to disclose, teach, or suggest each method step in the claims.

For convenience of analysis, independent claim 6, as amended, is repeated below in its entirety.

> 6. A method for performing single-instruction multiple-data instructions using a single multiply-accumulate unit, comprising the steps of:
> providing a multiply-accumulate unit configured to generate a first half of a data result and a second half of a data result;
> ***applying the first half of the data result at an input of a register***;
> using a miscellaneous-logic unit to generate an exception result; and
> ***applying the first half of the data result and the second half of the data result at an input of a buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are valid, otherwise applying an exception result at the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid.***

(Applicant's independent claim 6 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized method steps of pending claim 6 as shown above. Consequently, claim 6 is allowable.

First, as discussed above, the '257 patent fails to disclose, teach, or suggest, Applicant's claimed step of "***applying the first half of the data result at an input of a register***." In this regard, the Office Action mailed March 4, 2003 alleges that element

M3 is a register. Applicant respectfully disagrees. A register consists of a group of flip-flops and logic gates that effect their transition. The flip-flops hold binary information while the logic gates control when and how the binary information is transferred into the register. After data is stored in the register, the data can be "read" and/or applied multiple times to circuit elements coupled to the output of each respective flip-flop. Consequently, for at least the reason that a delay element is not a register, Applicant submits that the proposed combination of the '257 patent and the '652 patent fails to disclose, teach, or suggest Applicant's claimed step of "***applying the first half of the data result at an input of a register***." Accordingly, for at least this reason, claim 6 and each dependent claim that depends therefrom are allowable over the proposed combination of the '257 patent and the '652 patent.

Second, as acknowledged by the Office Action rejection of claim 4, the '257 patent is silent regarding detecting and reporting exception(s). To remedy this failure, the Office Action rejection alleges that one skilled in the art could reach the Applicant's claimed invention by combining the circuits allegedly taught in the '257 patent with exception detection and handling as taught in the '652 patent. Applicant respectfully disagrees.

The apparatus apparently disclosed in the '652 patent shows a plurality of exception detectors in a one-to-one relationship with a plurality of processing elements. When exceptions are indicated by the exception detectors, an exception signal is forwarded to a combining unit that generates a global exception from the one or more exception signals. Significantly, the '652 patent *does not* describe "***applying an exception result at the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid.***"

In contrast, Applicant's claimed invention recites "***applying the first half of the data result and the second half of the data result at an input of a buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are valid, otherwise applying an exception result at the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid.***" Neither the '257 patent nor the '652 patent disclose, teach, or suggest "***applying an exception result at the input of the buffer when the miscellaneous-logic unit determines that***

the first half of the data result and the second half of the data result are invalid." Consequently, even the proposed combination of the '257 patent and the '652 patent fail to disclose, teach, or suggest each method step recited in Applicant's claimed invention.

Accordingly, for at least these reasons, Applicant's claim 6 and each dependent claim that depends therefrom are allowable over the proposed combination of the '257 patent and the '652 patent. Applicant therefore requests that the rejection of claims 6-10 be withdrawn.

3. Claims 11 and 12

Applicant respectfully traverses the rejection of claims 11 and 12 under 35 U.S.C. §103(a) for at least the reason that even the proposed combination of references fails to disclose, teach, or suggest each element in the claims.

For convenience of analysis, independent claim 11, as amended, is repeated below in its entirety.

> 11. An apparatus for performing single-instruction multiple-data instructions, comprising:
> means for generating a first data result responsive to a first operand;
> ***means for storing the first data result***;
> means for generating a second data result responsive to a second operand;
> means for generating an exception result responsive to the first and second data results;
> ***means for forwarding the first data result and the second data result to a buffer when the exception result indicates that the first data result and the second data result are valid***; and
> ***means for communicating the exception to the buffer when the means for forwarding indicates that the first and second data results are invalid.***

(Applicant's independent claim 11 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized elements of pending claim 11 as shown above. Consequently, claim 11 is allowable.

In this regard, the Office Action rejection alleges that claim 11 does not recite limitations above the claimed invention set forth in claim 6. Applicant disagrees with

the rejection for at least the reason that the proposed combination of the '257 patent and the '652 patent fail to disclose, teach, or suggest each element recited in Applicant's claimed invention.

First, as discussed above, the '257 patent fails to disclose, teach, or suggest, Applicant's claimed "***means for storing the first data result***." For at least the reason that the delay element (M3) apparently disclosed in the '257 patent is not a register and is not capable of storing data, Applicant submits that the proposed combination of the '257 patent and the '652 patent fails to disclose, teach, or suggest Applicant's claimed "***means for storing the first data result***." Accordingly, for at least this reason, claim 11 and each dependent claim that depends therefrom are allowable over the proposed combination of the '257 patent and the '652 patent.

Second, as noted above, the '652 patent *does not* describe "***means for communicating the exception to the buffer when the means for forwarding indicates that the first and second data results are invalid***."

In contrast, Applicant's claimed invention recites "***means for forwarding the first data result and the second data result to a buffer when the exception result indicates that the first data result and the second data result are valid***; and ***means for communicating the exception to the buffer when the means for forwarding indicates that the first and second data results are invalid.***" Neither the '257 patent nor the '652 patent disclose, teach, or suggest "***means for forwarding the first data result and the second data result to a buffer when the exception result indicates that the first data result and the second data result are valid***; and ***means for communicating the exception to the buffer when the means for forwarding indicates that the first and second data results are invalid.***" Consequently, even the proposed combination of the '257 patent and the '652 patent fail to disclose, teach, or suggest each element recited in Applicant's claimed invention.

Accordingly, for at least these reasons, Applicant's claim 11 and claim 12 that depends therefrom are allowable over the proposed combination of the '257 patent and the '652 patent. Applicant therefore requests that the rejection of claims 11 and 12 be withdrawn.

CONCLUSION

In summary, Applicant respectfully requests that all outstanding claim rejections be withdrawn. Applicant respectfully submits that presently pending claims 1-12 are allowable and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response or intends to dispose of this matter in a manner other than a Notice of Allowance, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

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